AMENDMENT TO THE SPECIFICATION

Please amend the paragraph beginning on page 2, line 8 as follows:

--In order to overcome this problem, conventional semiconductor integrated circuit systems have achieved high-speed data transmission, while compensating clock skew by reducing a delay in signal transmission as a result of shortening the bus length between the memory controller and each memory device. One such semiconductor integrated circuit system has been disclosed in U.S. Patent 5,408,129 by Rambus. In this system, the distance between the memory controller and each memory device is shortened as shown in Figures 21(a) and 21(b) ~~17 (a) and 17 (b)~~ to achieve high-speed stable operation, and when a large number of memory devices are connected, the memory controller to be installed in the master chip is provided with a plurality of channels to control the memory devices.--

Please amend the paragraph beginning on page 12, line 18 as follows:

--Figure **2** shows the internal structure of the determination circuit **7**. As shown in the structure, the determination circuit **7** comprises an input unit **7a** which receives commands from the bus B, a determination unit **7b** which analyzes the received commands, a latch circuit **7c** which holds the determination results of the determination unit **7b** until it receives the next determination results, and an output unit **7d** [[**7b**]] which outputs the determination results transferred from the latch circuit **7c**. The behavior of the determination circuit **7** will be roughly described as follows. The determination unit **7b** generates the selector signal Sa, Sb or Sc activating the selector switch SWa, SWb or SWc, respectively, from the two higher order bits of a packet-mode command that the input unit **7a** has received. To be more specific, as shown in

Figure **3(c)**, the determination unit **7b** decodes the two higher order bits "01", "10" and "11" of the command so as to activate the respective selector switches SWa, SWb and SWc which correspond to the slave chips **2a**, **2b** and **2c** by generating the respective selector signals Sa, Sb and Sc. The selector signal Sa, Sb or Sc generated in the determination unit **7b** is maintained as it is in the latch circuit **7c** until the next selector signal is generated. The output unit **7d** receives the selector signal Sa, Sb or Sc from the latch circuit **7c** and outputs it to the selector circuit **8**. The determination circuit **7** can be arranged either independently as shown in Figure **1** or inside the selector circuit **8**. The selector signals Sa, Sb and Sc generated in the determination unit **7b** can be transmitted either via the transmission paths having plural bits as shown in Figure **2**, or via fewer transmission paths by serial-parallel converting the signals.--